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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/781,112	02/18/2004	Koucheng Wu	KWU002	1961

7590 07/12/2005

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/781,112	WU, KOUCHENG	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) *23-32* is/are withdrawn from consideration.

5)☐ Claim(s) *20-22* is/are allowed.

6)☒ Claim(s) *1-6 and 9-19* is/are rejected.

7)☒ Claim(s) *7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/18/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 02/18/2004 is acceptable.

Election/ Restriction

2. Applicant's election without traverse of Invention I, claims 1-22, in the reply filed on 06/25/2005 is acknowledged.

3. Claims 23-32 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 06/25/2005 as noted above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1-6 and 9-19** are rejected under 35 U.S.C. §103(a) as being unpatentable over Admitted Prior Art ("APA", disclosed in Figs. 1 through 5b of the present application and taught by Lin et al.).

Referring to **claim 1**, the APA discloses a semiconductor device having an electrically erasable programmable read only memory (EEPROM) substantially as claimed comprising:

a contactless array of EEPROM memory cells disposed in rows and columns (Fig. 2) and constructed over a silicon-on-insulator (SOI) wafer (10,11, Fig. 1), each EEPROM memory cell comprising a drain region (generally indicated as D), a source region (generally indicated as S), a gate region (12/13/14/15), and a body region (generally indicated as B);

a plurality of gate lines (WLx, Fig. 2) each connecting the gate regions of a row of EEPROM memory cells;

a plurality of body lines (BLx) each connecting the body regions of a column of EEPROM memory cells;

a plurality of source lines (SLx) each connecting the source regions of a column of EEPROM memory cells; and

a plurality of drain lines (DLx) each connecting the drain regions of a column of EEPROM memory cells;

wherein the source lines and the drain lines are buried lines.

However, the APA fails to teach that the source regions and the drain regions of a column of the EEPROM cells are insulated from the source regions and the drain regions of the adjacent columns of the EEPROM cells, otherwise known as an EEPROM NOR array in the art. In the APA, the source regions and the drain regions of a column of the EEPROM cells are electrically connected to the source regions and the drain regions of the adjacent columns of the EEPROM cells (Fig. 2), otherwise known as an EEPROM NAND array in the art.

Nevertheless, the difference between an EEPROM NOR array and an EEPROM NAND array is well established in the art: an EEPROM NOR array offers higher speed but with more chip space than an EEPROM NAND array; whereas, an EEPROM NAND array provides compact size but with a slower speed; and the ability to choose between the two designs, as a matter of suitable (intended) use, is well within the skill of an artisan of ordinary skill in the art, therefore such ability to choose, which leads to such change, would have been obvious at the time the invention was made (see, for example, Kim et al., U.S. Patent Application Publication 20040097044, paragraph [0005]).

Referring to **claims 2-5**, the APA furthers discloses that the gate (12/13/14/15) is a stacked gate structure on the SOI wafer, including a control gate region 15, a floating region 13 separated from the control gate region by an insulating layer 14, the floating region being disposed over the body region and separated from the body region by an insulating layer, where the insulating layer is a silicon oxide film.

Referring to **claim 6**, the use of one or more oxide layers for the purpose of insulating source and drain regions are known in the art, therefore such usage would have been obvious.

Referring to **claim 9**, the APA's figures depict that the drain region and the source region in one or more of the EEPROM memory cells are disposed in a substantially symmetric structure relative to the gate region and the body region.

Referring to **claim 10**, the APA's figures depict that the body region comprises a semiconductor material of a first conductivity type (p), and the source region and the drain region comprise a semiconductor material of a second conductivity type (n) that is opposite to the first conductivity type.

Referring to **claims 11-19**, applying different voltages at the gate lines and other conductive lines to operate the EEPROM cells was within the skill of a person of ordinary skill in the art, therefore such operating procedures are not patentable.

Allowable Subject Matter

5. Claims 20-22 are allowable over the prior art of record.

Claims 7-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a semiconductor device having an electrically erasable programmable read only memory (EEPROM) with all exclusive limitations as recited in claim 7 or claim 20, characterized in that at least one source line of a column of EEPROM memory cells is electrically connected to the body line of the same column of EEPROM memory cells (claim 7) or that a plurality of source lines each connecting the source regions and the body regions of a column of EEPROM memory cells (claim 20).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
July 08, 2005